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Application / Conf. No.	10/812,550 / 3439
Filing Date	March 29, 2004
First Named Inventor	Rajat Aggarwal
Art Unit	2825
Examiner Name	Paul Dinh
Attorney Docket Number	X-1490 US

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PD		Hiroshi Murata et al.; "VLSI Module Placement Based on Rectangle-Packing by the Sequence-Pair, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 15, No. 12; December 1996; Copyright 1996 IEEE; pp. 1518-1524.					
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